

This Page Is Inserted by IFW Operations  
and is not a part of the Official Record

## **BEST AVAILABLE IMAGES**

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

IMAGES ARE BEST AVAILABLE COPY.

**As rescanning documents *will not* correct images,  
please do not report the images to the  
Image Problems Mailbox.**

**THIS PAGE BLANK (USPTO)**

# (12) UK Patent Application (19) GB (11) 2 164 828 A

(43) Application published 26 Mar 1986

(21) Application No 8523031

(22) Date of filing 18 Sep 1985

(30) Priority data

(31) 653743

(32) 21 Sep 1984

(33) US

(71) Applicant

International Standard Electric Corporation  
(USA-Delaware),  
320 Park Avenue, New York 10022, State of New York,  
United States of America

(72) Inventor

Hyokang Chang

(74) Agent and/or Address for Service

J C Vaufrourard,  
ITT Patent Department UK, Maidstone Road, Fooks Cray,  
Sidcup DA14 5HT

(51) INT CL<sup>4</sup>

H04B 3/23

(52) Domestic classification

H4R LES

(56) Documents cited

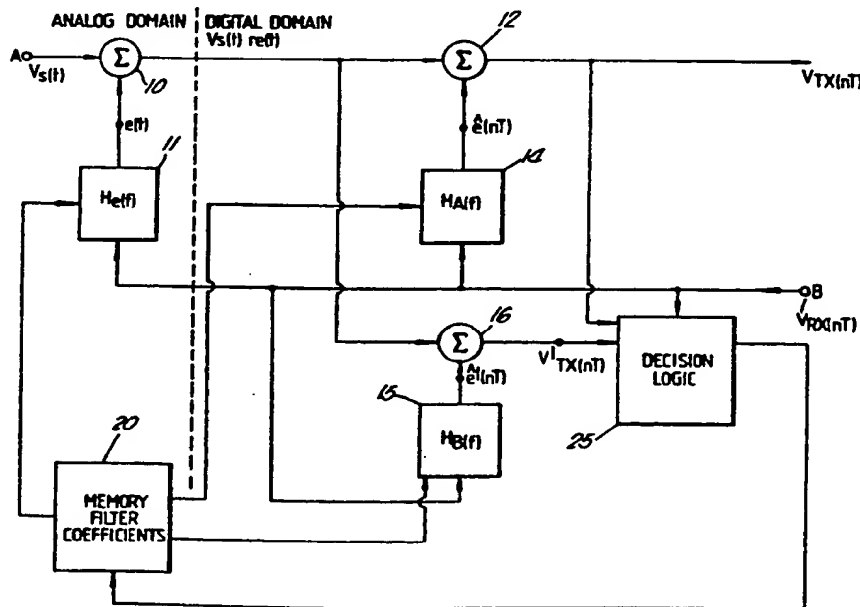
US 3787645

(58) Field of search

H4R

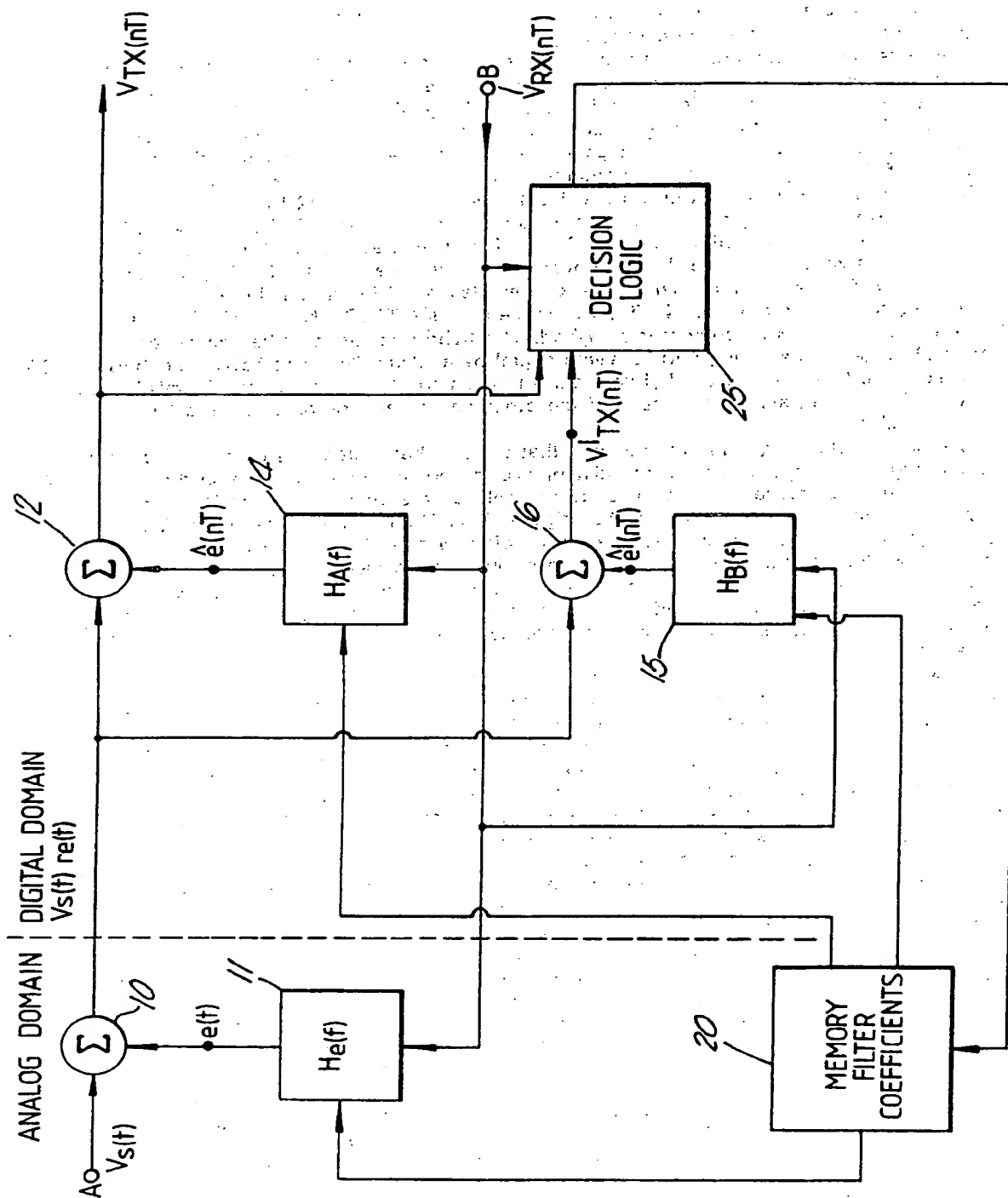
## (54) A method of reducing echo in a digital switching system and a digital hybrid therefor

(57) A method and digital hybrid circuit apparatus is disclosed for connecting a near end subscriber to a far end subscriber with the near end subscriber providing a digital input signal  $V_s$  which undesirably contains an interfering echo signal  $e(T)$ . This signal is transmitted to a connected far end subscriber which far end subscriber provides a far end digital input signal  $V_{RX}$  for reception by the near end subscriber. In order to eliminate the echo signal, first  $H_A(f)$  and second  $H_B(f)$  programmable coefficient digital filters have an input to receive the far end digital signal with the outputs of the filters coupled to an input of an adder 12, 16 with one input of each adder to receive the near end input signal, means 20 is provided for programming each of the filters with a different set of coefficients and logic means 25 are coupled to the output of the adders for comparing the average power output of each of the adders and means for selecting that filter and adder which provides the lowest value of average power and to employ those coefficients in filter  $H_A(f)$  to thereby provide an output signal to be transmitted to the far end subscriber which contains a minimum level of the interfering echo signal.



GB 2 164 828 A

//



## SPECIFICATION

**A method of reducing echo in a digital switching system and a digital hybrid therefor**

5 The present invention relates to telephone line circuits in general and more particularly to a digital hybrid for use in a telephone line circuit. 5

with the advent of digital exchanges in the local telephone network, there is a need for better and more accurate balancing of the hybrid used for 2- to 4-wire conversion than those used in analog exchanges because of the 4 wire switching nature of digital exchanges.

10 As one can ascertain, the digital exchange has been widely employed due to the fact that such exchanges can handle both analog and digital data, and furthermore by utilizing digital techniques, many of the components of such systems can be integrated. An example of a widely employed digital communication system is designated as the ITT 1240 Digital Exchange. 10

Such systems employ 4-wire lines whereby two lines are used for transmission and two lines for reception. In any event, a subscriber line is a 2-wire line. The lines are used to simultaneously transmit and receive. Hence, in order to convert the 2-wire line to a 4-wire line, a hybrid is employed. Such hybrids are well known and have been described in many publications. 15

See for example, our U.S. Patent No. 4,161,633 entitled SUBSCRIBER LINE/TRUNK CIRCUIT. That patent shows a 2- to 4-wire converter or hybrid. The hybrid circuit must be accurately balanced especially when transmitting and receiving digital data. Basically, there have been two approaches to accurate balancing of the hybrid—one to select the best one out of M available balance networks for a given subscriber line, and the other one to employ an automatically adaptive echo canceller. 20

As one can ascertain, the magnitude of the echo that a talker hears depends on the echo path loss. This is the sum of the return loss at the distant hybrid and the round trip loss in the circuit. The subscriber's tolerance of echo depends not only on the echo magnitude but also on the round trip delay between the echoes and the original signal. Immediate echos sound like sidetone, but longer delayed echoes are extremely disturbing. Hence, if the delay cannot be reduced, and if return loss at the hybrids is improved by impedance balancing, there is only one more commonly known way to make the echo tolerable. Thus, in certain conventional techniques, the echo magnitude was decreased by increasing the electrical loss by the talker and the point where the mismatch occurs. This, of course, reduces received volume and is a completely unacceptable approach. 25

In the more modern approaches as indicated above, in order to select one out of M balancing networks, the system engineers must measure the subscriber line characteristic in order to make a decision as to which one to select. The use of the adaptive echo canceller was attractive in the sense that it did not require measurement of the subscriber line characteristic and it provided an accurate balancing. However, it is extremely expensive due to the fact that it constitutes a relatively complicated circuit and one such circuit has to be included in each subscriber line. 30

Thus the problem of eliminating echos with the use of the adaptive echo canceller provides satisfactory results but is an expensive way of implementation. 40

The previously mentioned patent offers a solution which employs digital filters. Therein any reflected signals are eliminated by a digital filter and a digital subtraction technique that is implemented under the control of a microprocessor wherein the return signal is continuously subtracted from the sum of the forward and return signals to eliminate undesired reflection signals which signals are primarily responsible for echoes. 45

Accordingly, the present invention seeks to provide a hybrid balancing scheme which is based upon a semi-automatic balancing approach. The concept of the approach is to select the best one out of M available balance networks in a semi-automatic process. This approach obviates the need for measurement of the subscriber line characteristics. The implementation of M balance networks is accomplished by employing a programmable digital filter referred to as a digital hybrid and which has M sets of filter coefficients. 50

The use of digital filters is extremely well known. A description of the general design of such filters may be found in a text entitled DIGITAL PROCESSING OF SIGNALS, B. Gold and C. Rader, Lincoln Lab Publication, McGraw-Hill, 1969. Essentially, a digital filter employs multipliers, adders and basic delay elements to implement a given transfer function. The design of such filters as employed in telephone line circuits is well known as is the nature of the echo signals. 55

According to a first aspect of the invention there is provided a digital hybrid apparatus for use in a line circuit employed in a digital switching network for connecting a near end subscriber to a far end subscriber, in which the near end subscriber provides a digital input signal which contains an interfering echo signal for transmission to a connected far end subscriber which far end subscriber provides a far end digital input signal for reception by the near end subscriber, the apparatus comprising first and second programmable coefficient digital filters each having one input which is adapted to receive the far end digital signals, the outputs of which filters are coupled to an input of an associated adder and another input of each adder is adapted to 60

65 coupled to an input of an associated adder and another input of each adder is adapted to 65

receive the near end input signal, means for programming each of the filters with a different set of coefficients, logic means coupled to the output of the adders for comparing the average power output of each of the adders and means for selecting that filter and adder such that the set of coefficients provides the lowest value of average power.

5 According to a second aspect of the invention there is provided a digital hybrid apparatus for use in a line circuit employed in a digital switching network for connecting a near end subscriber to a far end subscriber, in which the near end subscriber provides a digital input signal which undesirably contains an interfering echo signal for transmission to a connected far end subscriber which far end subscriber provides a far end digital input signal for reception by the near end subscriber, comprising a first programmable digital filter means having an input for receiving the far end digital signal, means for providing at an output a first filtered signal indicative of the interfering echo signal, a first adder having one input responsive to the near end digital input signal, and a second input coupled to the output of the first digital filter to provide at an output of the first adder a first signal indicative of the difference between the input signals, a second programmable digital filter means having an input for receiving the far end digital signal, means for providing at an output a second filtered signal indicative of the interfering echo signal, a second adder having one input responsive to the near end digital input signal and a second input coupled to the output of the second digital filter to provide at an output of the second adder a second signal indicative of the difference between the input signals, means for changing the coefficients, the means being coupled to the first and second programmable filters to program the coefficients associated with each of the filters, logic means coupled to the outputs of the first and second adders to compare the values of the first and second signals to select a set of coefficients from the first or second filter which provides the closest approximation to the echo signal, and means for programming the selected coefficients into one of the first or second filters.

According to a third aspect of the invention there is provided a method of reducing the interfering effect of an echo signal generated by a connection between a near end subscriber and a far end subscriber in a digital switching system wherein the near end subscriber provides a digital input signal which contains the echo signal for transmission to the far end subscriber which far end subscriber provides a far end digital input signal for reception by the near end subscriber, the method comprising the steps of applying the far end digital input signal to the inputs of first and second programmable digital filters, summing each of the outputs of the first and second programmable filters with the near end digital signals, programming the first and second filters with a set of M different coefficients, comparing the summed outputs of the first filter with the second filter for each of the M coefficients, and selecting the summed output of the first or second filter which provides the lowest signal power level to select one of the M coefficients for one of the filters.

In order that the invention and its various other preferred features may be understood more easily, an embodiment thereof will now be described, by way of example only, with reference to the drawing, the single figure of which is a block diagram of a digital hybrid apparatus embodying the principles of the present invention.

The intention of the hybrid circuit is to cancel or reduce the echo signal as previously mentioned. This is particularly important in digital systems, as previously explained, and it is further desirable to reduce or cancel the echo signal without introducing additional attenuation between near end and far end subscribers.

Referring to the drawing, an input terminal A receives an input signal from a near end talker or near end subscriber. The input signal from the near end subscriber is applied to one input of an adder 10. Another input to the adder 10 is obtained from a digital filter 11 which is a programmable filter. Programmable digital filters are well known in the art and are designated as programmable filters due to the fact that the filter coefficients or constants can be changed or programmed according to the desires of the user.

Shown in the drawing is a memory module 20. The memory module, which may be part of the filter, serves to store filter coefficients for the programmable filter, such as filter 11, and to change the filter coefficients according to an instruction command or according to a digital word impressed upon the input of the filter.

The output from the filter 11 is the echo signal designated as e(T). As can be seen from the drawing, the input signal at terminal A will have impressed thereon a signal which is the echo signal and which signal unduly interferes with the input signal according to the well known effects of the echo. The output from the adder 10 is impressed upon the input of an additional adder 12. The adder 12 has another input receiving a signal from a primary programmable digital filter 14. The digital filter 14, as indicated, is also programmable and has its coefficients applied to the filter from the memory 20. The inputs to digital filters 11 and 14 are derived from terminal B which is the digital input signal from the far end subscriber.

A third programmable filter 15 is also shown and, is in parallel with filter 14. The digital filter 15 is also programmable and is associated with an adder circuit 16. A first input to the adder

16 is from the output of adder 10. The second input is from the digital filter 15. The output from the adder 16 is applied to the input of a decision logic module 25 which also receives the output from adder 12.

The output of adder 12 is the digital output signal at the transmit side of the line which is the signal emanating and due to the primary hybrid filter 14. Each filter is designated by a general transfer characteristic such as filter 11  $H_o(f)$ , filter 14  $H_A(f)$  and filter  $H_b(f)$ . As will be explained, the circuit functions such that the decision logic 25 selects the filter coefficients for the primary filter 14 such that the selected coefficients reduce the echo signal in an optimum manner. The decision logic 25 operates to monitor the outputs of filter 14 and filter 15 as applied via the adders, 12 and 16, to then determine which filter provides the closest approximation to the actual error signal.

Upon determining this, the decision logic then causes those coefficients to be used in the primary filter 14 for processing of the signal and to substantially reduce echo interference. As seen in the drawing, the various signals at pertinent points in the circuit are indicated on the diagram. The operating principle of the components shown in the drawing is as follows. The description given below is a mathematical analysis of the operation of the structure shown in the drawing where the relationships as designated in the drawing are given as follows:

$V_{RX}(nT)$ : Digital input signal from the far-end taker  
 $V_{TX}(nT)$ : Digital output signal at the transmit side right after the primary hybrid filter  $H_A(f)$   
 $e(T)$ : Echo signal  
 $V_s(T)$ : Input signal from the near-end talker  
 $\hat{e}(nT)$ : Digital echo estimate from  $H_A(f)$   
 $V'_{TX}(nT)$ ,  $\hat{e}'(nT)$ : Digital output signal and echo estimate with the secondary hybrid filter  $H_b(f)$

The signal  $V_{TX}$  is then given by:

$$V_{TX}(nT) = V_s(nT) + (e(nT) - \hat{e}(nT)) = V_s(nT) + r(nT)$$

where  $r(nT)$  represents the residual echo signal (or, in other words, the leakage of  $V_{RX}(nT)$ ). The objective of the digital hybrid is to produce an echo estimate,  $\hat{e}(nT)$ , as close to  $e(T)$  as possible.

In this manner the adder 12, which is a subtractive adder, subtracts the echo signal developed at the output of filter 14 from the signal applied to the input of the adder 12 and hence substantially reduces the echo signal accordingly. Since  $V_s(nT)$  and  $V_{RX}(nT)$  are two independent signals, so are  $V_s(nT)$  and  $r(nT)$  and hence there is no correlation between them. Consequently, the mean-squared level of  $V_{TX}$  is given by

$$\bar{V}_{TX}^2 = \bar{V}_s^2 + \bar{r}^2$$

Hence, the optimum choice of the hybrid coefficients set can be made by selecting one which minimizes  $\bar{V}_{TX}^2$  the average power at the transmit side, since  $\bar{V}_s^2$  is not affected by the choice.

In an adaptive approach, the coefficients of the digital hybrid are continuously updated in a direction to minimize  $\bar{V}_{TX}^2$  through the computation of a gradient vector composed of  $L$  cross-correlations between the transmit signal and time-delayed receive signals appearing at  $L$  filter taps. But in this application, instead of updating individual filter coefficients, the circuit simply compares the results from two different sets of coefficients and gives an indication of which one to select. With this indication, the supervising software can maintain the set of coefficients selected thus far in the primary hybrid filter and continue the comparison by loading a new set of coefficients in the second hybrid filter until it exhausts  $M$  prescribed coefficient sets.

#### Decision Logic

On denoting  $V_{TX}(nT)$  by  $y(n)$  and  $y'(n)$ , respectively, the corresponding average signal power levels are given by:

$$P = \overline{V_{TX}^2} = \frac{1}{N} \sum_{n=0}^{N-1} [y(n)]^2$$

$$P' = \overline{V_{TX}'^2} = \frac{1}{N} \sum_{n=0}^{N-1} [y'(n)]^2$$

where  $N$  is the number of samples to average over. The selection algorithm for the new digital hybrid is then given as follows:

Select  $H_A(f)$  if  $(P-P')/P \geq d$  where  $d$  is a fixed threshold level ( $d \geq 0$ ). Otherwise, select  $H_A(f)$ .

Now let us consider one way to implement the above selection algorithm. Note that

$(P-P')/P \geq d$  is equivalent to:

$$P - P' \geq dP$$

$$(1-d)P - P' \geq 0$$

$N-1$

$$\sum_{n=0}^{N-1} [\sqrt{1-d} y(n) + y'(n)][\sqrt{1-d} y(n) - y'(n)] \geq 0$$

for  $d \ll 1$ ,  $\sqrt{1-d} \approx 1 - 1/2d$

The above expression is again equivalent to:

$N-1$

$$\sum_{n=0}^{N-1} [y(n) - 1/2d y(n) + y'(n)][y(n) - 1/2d y(n) - y'(n)] \geq 0$$

$$y'(n) \geq 0$$

By constraining  $d$  to be of the form  $2^{-k}$ , it finally becomes:

$N-1$

$$\sum_{n=0}^{N-1} [y(n) - 2^{-(k+1)} y(n) + y'(n)][y(n) - 2^{-(k+1)} y(n) - y'(n)] \geq 0$$

$$y(n) - y'(n) \geq 0$$

Like adaptive echo cancellers, the semi-automatic digital hybrid depends on the incoming speech signal in making a binary selection decision. The above comparison is therefore valid only if the "quality" of the incoming signal exceeds a certain threshold level. For example, the best signal to be expected for the selection purpose is a white noise and the worst a single tone.

Furthermore, the incoming signal should not be corrupted by the signal or noise from the near-end talker side.

On denoting:

$$u = (1/N) \sum_{n=0}^{N-1} |V_{RX}(nT)|$$

$$u_p = \max_{0 \leq n \leq (N-1)} |V_{RX}(nT)|$$

$$v = (1/N) \sum_{n=0}^{N-1} |V_{TX}(nT)|$$



The conditions under which the comparison between the primary and secondary hybrid filters is valid are given as follows:

- (i) check for minimum level:  $u \geq u_0$
- (ii) check for signal bandwidth:  $u_p \geq \lambda_1$

- 5 (iii) check for double talking:  $v < \lambda_2 u$

where  $u_0$ ,  $\lambda_1$  and  $\lambda_2$  are threshold parameters. Initially,  $\lambda_1$  and  $\lambda_2$  may be set to two and one respectively.

Having made the comparison and checked the validity of the incoming signal, the decision logic gives an indication of one of the following three states:

- 10 (i) State P: Comparison complete; update the coefficients of the primary filter with those of the secondary one.

(ii) State N: Comparison complete; no updating needed.

(iii) State Z: Comparison incomplete; wait until comparison is completed.

As can be seen from the above, the decision logic is a relatively simple circuit which can be easily implemented by a microprocessor. The format to be followed based on the above can be implemented by many software programs within the scope of those skilled in the art.

Essentially, the decision logic circuit 25 operates as follows. The decision logic circuit compares the output signal from adder 16 with the output signal from adder 12. If the signal from adder 16 is greater than the signal from adder 12, it will then command the memory 20 to load the next set of coefficients into filter 15. This essentially is the operation described in conjunction with State P. In State N there is no updating required which means that after comparison, the output from adder 12 is less than the output from adder 16 which means that the coefficients in filter 14 are closer to the desired values than the coefficients in filter 15. Hence during State N, a new state of coefficients is again loaded into filter 15. In the State Z the comparison is incomplete and hence the system does not change filter coefficients until a comparison is complete.

After the complete set of coefficients, as stored in memory 20, has been exhausted, the decision logic instructs the memory module 20 to insert those coefficients in filter 14 which result in the lowest echo signal. The system operates on a realtime basis, and hence the coefficients are constantly being changed whereby the filter 14 will always have impressed thereon the optimum set of coefficients based on the particular signal received.

The above noted checks regarding level bandwidth and double talking, as above indicated, are also implemented by the decision logic circuit which again, as indicated, may be a software program which essentially solves the above noted equations.

As seen, the decision logic has impressed upon inputs the digital input signal from the far end subscriber as well as the digital output signal from the near end subscriber.

Hence the above noted equations can be solved based on the conditions specified above. Therefore, the above comparison is valid due to the fact that the decision logic circuit 25 checks the validity the incoming signal before indicating one of the three possible states.

The improved digital hybrid consists of two identical digital filter blocks, each of which is programmable and each of which interfaces with a decision logic block. The filter blocks are loaded with two different sets of hybrid coefficients and the decision logic will provide an indication of which filter to select. This feature enables the supervising software to select the best one out of the M available coefficient sets under normal operating conditions as when a call is in progress. The decision logic operates to compare the two sets of coefficients at a time and, as will be explained, selects the best set of coefficients and uses that set to specify the characteristics of the programmable filter.

#### CLAIMS

50 1. A digital hybrid apparatus for use in a line circuit employed in a digital switching network for connecting a near end subscriber to a far end subscriber, in which the near end subscriber provides a digital input signal which contains an interfering echo signal for transmission to a connected far end subscriber which far end subscriber provides a far end digital input signal for reception by the near end subscriber, the apparatus comprising first and second programmable coefficient digital filters each having one input which is adapted to receive the far end digital signals, the outputs of which filters are coupled to an input of an associated adder and another input of each adder is adapted to receive the near end input signal, means for programming each of the filters with a different set of coefficients, logic means coupled to the output of the adders for comparing the average power output of each of the adders and means for selecting that filter and adder such that the set of coefficients provides the lowest value of average power.

2. An apparatus as claimed in claim 1, wherein the filter programming means includes a memory for storing therein a set of M filter coefficients of the filters.

3. An apparatus as claimed in claim 1 or 2, wherein one of the adders is used to connect to the far end subscriber.

4. An apparatus as claimed in claim 3, wherein the filter associated with the other adder is programmed with the M coefficients, the logic means including means for transferring the selected coefficients to the other filter associated with said one of the adders.

5. a digital hybrid apparatus for use in a line circuit employed in a digital switching network for connecting a near end subscriber to a far end subscriber, in which the near end subscriber provides a digital input signal which undesirably contains an interfering echo signal for transmission to a connected far end subscriber which far end subscriber provides a far end digital input signal for reception by the near end subscriber, comprising a first programmable digital filter means having an input for receiving the far end digital signal, means for providing at an output a first filtered signal indicative of the interfering echo signal, a first adder having one input responsive to the near end digital input signal, and a second input coupled to the output of the first digital filter to provide at an output of the first adder a first signal indicative of the difference between the input signals, a second programmable digital filter means having an input for receiving the far end digital signal, means for providing at an output a second filtered signal indicative of the interfering echo signal, a second adder having one input responsive to the near end digital input signal and a second input coupled to the output of the second digital filter to provide at an output of the second adder a second signal indicative of the difference between the input signals, means for changing the coefficients, the means being coupled to the first and second programmable filters to program the coefficients associated with each of the filters, logic means coupled to the outputs of the first and second adders to compare the values of the first and second signals to select a set of coefficients from the first or second filter which provides the closest approximation to the echo signal, and means for programming the selected coefficients into one of the first or second filters.

6. An apparatus as claimed in claim 5, wherein the coefficient changing means comprises a memory having stored therein a set of coefficients for each of the first and second filters.

7. An apparatus as claimed in claim 5 or 6, wherein the logic means is operative to compare the effective power of the first and second signals to select the coefficients according to the minimum power level contained in the first and second signals.

8. An apparatus as claimed in any one of claims 5 to 7, wherein the selected coefficients are programmed into the first filter in accordance with the output of the first adder coupled to the far end subscriber.

9. An apparatus as claimed in any one of claims 1 to 4 or 8, wherein the comparison of power is implemented according to the following relationship:

$$p - p' \geq d$$

where

p = average power from signal at output of a first adder;

p' = average power from signal at output of a second adder; and

d = a threshold level greater than zero.

10. A digital hybrid apparatus substantially as described herein with reference to the drawing.

11. a method of reducing the interfering effect of an echo signal generated by a connection between a near end subscriber and a far end subscriber in a digital switching system wherein the near end subscriber provides a digital input signal which contains the echo signal transmission to the far end subscriber which far end subscriber provides a far end digital input signal for reception by the near end subscriber, the method comprising the steps of applying the far end digital input signal to the inputs first and second programmable digital filters, summing each of the outputs of the first and second programmable filters with the near end digital signals, programming the first and second filters with a set of M different coefficients, comparing the summed outputs of the first filter with the second filter for each of the M coefficients, and selecting the summed output of the first or second filter which provides the lowest signal power level to select one of the M coefficients for one of the filters.

12. A method as claimed in claim 11, wherein the step of comparing the outputs of the first and second filters includes the step of calculating the power output of the first and second summed signals, comparing the power levels according to:-

$$p - p' \geq d$$

where

p = power level of the first summed signal,

p' = power level of the second summed signal,

d = threshold constant greater than zero, and selecting the lower of said power levels to specify said first or second filter coefficients.

13. A method as claimed in claim 12, including the steps of first checking the far end input signal for level according to whether  $u \geq u_0$ , based on the following relationship:

$$\mu = (1/N) \sum_{n=0}^{N-1} |v_{RX}(nT)|$$

5

wherein N is a positive integer greater than one.

14. A method as claimed in claim 13, including the step of checking the signal bandwidth according to whether  $u_p \geq \lambda_1 u$  based on the following relationship:

10

$$u_p = \max_{0 \leq n \leq N-1} |v_{RX}(nT)|$$

15

where  $\lambda_1$  = a positive integer.

15. A method as claimed in claim 14, including the step of further checking for double talking according to whether  $v < \lambda_2 v$  based on the following relationship:

20

$$v = (1/N) \sum_{n=0}^{N-1} |v_{TX}(nT)|$$

25

wherein

$\lambda_2$  = a positive integer.

30 16. A method of reducing the effect of an echo signal in a digital switching system substantially as described herein.

30

**THIS PAGE BLANK (USPTO)**